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New Products

INFORMATION

1

World's first 8GB, Speed Class 4 SDHC Memory Card

Toshiba Introduces World's Highest Class of SDHC Card to the World Market

Toshiba announced the global launch of the latest addition to its new series of high-capacity SDHC Memory Cards: the industry's first 8-gigabyte Class 4 memory card. The new card will be introduced in January 2007, alongside the 4GB products launched in September 2006, and will give Toshiba a larger commercially available lineup in high performance SD Memory Cards.

The SDHC (SD High Capacity) Memory Card is based on the SD Card Association's SD Specifications Ver2.00, which defines high capacity, high performance enhancements to market-leading SD Memory Cards. The new card meets the Class 4 standard, a speed standard that requires a data write speed of at least 4MB a second. Toshiba is first in the industry to announce the launch of Class 4 8GB SDHC memory cards.

SDHC Memory Cards are expected to find wide application in digital video and still cameras, and Toshiba is enhancing global distribution of its new cards.

Features

❶8GB capacity supports capture of video images and high-resolution still images. The new card can record a maximum of 3hrs. 10mins. of standard definition video in the MPEG2 format.

❷Meets Class 4 in the "SD Speed Class", requiring high-speed writing of at least 4MB per second, up to 6MB per second.

■Specifications

Product Name	SD-HC008GT4
Capacity	8GB
SD Speed Class	Class 4
Maximum Write Speed	6MB / Second
Power Supply Voltage	2.7 - 3.6V
Compatible Standard	SD Memory Card Ver2.00 standard compatible
File Format	FAT32
Exterior Dimensions	24mm(W)x32mm(L)x2.1mm(T), Weight Approx. 2g

* The product name above is only for the Japanese market.
* Reading and writing speed depends on conditions such as devices and file size.
* SDHC Memory Card cannot be used for devices which do not support SD Memory Card Ver2.00 standard as the file formats differ.

INFORMATION

Toshiba, Sony and NEC Electronics Unveil Mass Production Platform Technology for 45nm Generation High Performance System LSI

Toshiba Corporation, Sony Corporation and NEC Electronics Corporation announced the successful co-development of an LSI mass production platform for next-generation 45 nanometer (nm) process technology. The new platform integrates elemental breakthroughs with cutting-edge technologies to achieve a highly efficient process for production of high performance system LSI. This technology was unveiled at the 2006 International Electron Devices Meeting (IEDM) in San Francisco, CA, U.S.A. in December.

The key elements of the new platform are a fully renovated MOSFET integration scheme, and a hybrid structure with a low dielectric constant (low-k) film that assures high performance and reliability.

The MOSFET integration process applies strained silicon technology to the transistor, utilizing crystal lattice distortion to induce performance-boosting local strain at key locations. Optimization of the strain boosts transistor performance to a level 30% faster than that achieved in the present generation of technology.

Application of a low-k film in the intermediate metal layer of the chip during the back-end process reduces parasitic capacitance and improves circuit performance. The three partners confirmed a dielectric gate film with an effective 15-year lifetime, a span surpassing the average lifetime of a high performance LSI. They also carried out exhaustive tests of the platform and proved a layer yield of over 98% for the challenging back-end process, confirming that the technology achieves the reliability essential for mass production.

In addition, the partners have led the industry in applying immersion lithography technology with an ultra-high numerical aperture (NA) of over 1.0 to formation of the transistor node, achieving a cell with an area of 0.248 micron m^2 in an ultra high density SRAM. The new cell is the smallest yet achieved.

The three companies are simultaneously developing two 45nm processes -- the current platform, which is ideal for high performance LSIs, as well as a platform for applications with low power consumption requirements, which is expected to be completed in early 2007.

■Outline of development

The high performance 45nm platform technology optimizes a balance of high performance and high reliability while combining individual elemental technology with new technologies and improvements. The specific technology elements are as follows.

1. Optimal processing conditions based on basic technology

(1) Optimizing application of strained silicon technology

Strained silicon technology enhances carrier mobility. In the new process, stress film is formed on the source/drain integration as well as the upper part of the transistors, a solution that enhances the strain effect and contributes to optimized transistor performance. The result is an improvement of over 30% in transistor performance as a whole, with an improvement in transistor drive current of over 20% and 60% in the nMOS and pMOS transistor modes, respectively.

(2) Optimizing back-end process technology

In the back-end process, the LSI interconnect layer is formed with a hybrid dual-damascene structure, with optimized porous low-k films applied to both the interconnect layer and the via layer. This approach enhances control of the interconnect profile. Optimization of the manufacturing process achieves an effective dielectric constant (keff=2.7) at the level required for 45nm generation performance. Tests have confirmed a layer yield of more than 98%, an excellent level on a test structure, matching actual production, and also confirmed circuit performance reliability.

[Application of strained silicon technology and performance improvement]

	Upper transistor part	Source and drain part	Improvement against current drive performance	Drive current
nMOS	High stress tensile liner	Stress Memorization Technique (SMT)	more than 20%	1100µA/µm (Ion) 100nA/µm (Ioff)
pMOS	High compressive liner	Embedded Silicon Germanium (eSiGe)	more than 60%	700µA/µm (Ion) 100nA/µm (Ioff)

2. High accuracy processing with ultra high NA immersion lithography

The companies confirmed the effectiveness of applying ultra high NA (over 1.0) immersion lithography. Contact holes were accurately controlled and formed to the expected size on an ultra-high-density SRAM (UHD-SRAM), meeting highly demanding tolerances for the LSI's internal structure. The process confirms that there are no problems with accuracy in applying ultra high NA immersion lithography to every circuit.

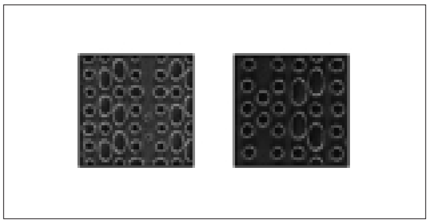


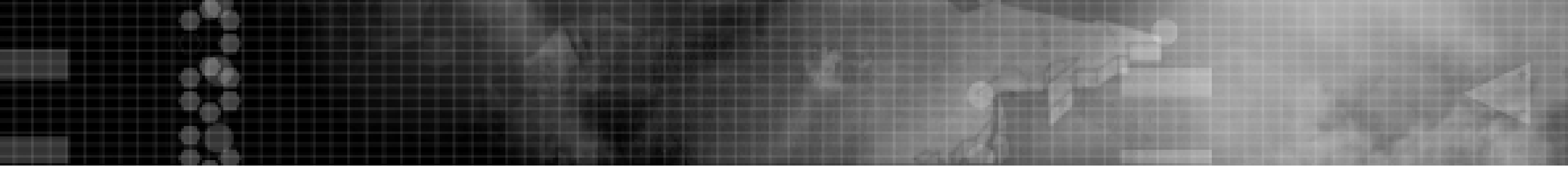
Fig. Contact holes on an UHD-SRAM processed with dry lithography vary widely (left), whereas there are few variations with ultra high NA immersion lithography (right).

Note:

*1:Strained silicon technology enhances the carrier mobility of transistor devices by utilizing crystal lattice distortion. A primary method is inducing local strain that forms a stress liner on top of transistor elements. In MOSFET, tensile stress and compressive stress are added to the nMOS and to pMOS, respectively.

*2:Low-k film is a low-dielectric-constant film used in the back-end process after forming transistors in the LSI manufacturing process. It reduces parasitic capacitance between the interconnect layers and so enhances performance. In general, low-k materials can cause deterioration in device solidity and are difficult to manufacture.

*3:Immersion lithography technology is a resolution enhancement technique that interposes a liquid medium between the optics and the wafer surface, replacing the usual air gap. It increases the numerical aperture (NA) of lens to a value greater than one, the limit that can be achieved with an air gap.



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