

**TOSHIBA Microcontrollers**  
**900 Family**  
**(TMP93CS20) (TMP93PW20A)**  
**(TMP93PS44) (TMP93CU44) (TMP93PW44A) (TMP93CW44) (TMP93CS44/45)**

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## Datasheet Modifications: I<sup>2</sup>C Bus Mode Control

The following modifications (shown in red) will be made to the technical datasheets in the next revision.

### Section: "I<sup>2</sup>C Bus Mode Control"

▪ **In the explanation of the Serial Bus Interface Control Register 1**

1. Delete the setting examples where the serial clock frequency exceeds 100 kHz.
2. Add the following note.

Serial clock selection

000	N = 4	- (Note)	$\left( \begin{array}{l} \text{System clock: } f_c \\ \text{Clock gear : } f_c/1 \\ f_c = 20 \text{ MHz} \\ \text{(Output on SCL pin)} \end{array} \right)$
001	N = 5	- (Note)	
010	N = 6	- (Note)	
011	N = 7	74.6 kHz	
100	N = 8	38.2 kHz	
101	N = 9	19.3 kHz	
110	N = 10	9.71 kHz	
111		Reserved	

**Note:** This I<sup>2</sup>C bus circuit does not support the Fast mode. It supports the Standard mode only. Although the I<sup>2</sup>C bus circuit itself allows the setting of a baud rate over 100 kbps, the compliance with the I<sup>2</sup>C specification is not guaranteed in that case.

▪ **In "(3) Serial clock"**

1. Add the following sentence about the communication baud rate.

a. Clock source

SBICR1<SCK2:0> are used to select a maximum transfer frequency output on the SCL pin in the master mode. **Set a communication baud rate that meets the I<sup>2</sup>C bus specification, such as the shortest pulse width of t<sub>LOW</sub>, based on the equations shown below.**

$$\begin{aligned}
 t_{\text{LOW}} &= 2^n / f_{\text{FPH}} \\
 t_{\text{HIGH}} &= 2^n / f_{\text{FPH}} + 12 / f_{\text{FPH}} \\
 f_{\text{scl}} &= 1 / (t_{\text{LOW}} + t_{\text{HIGH}}) \\
 &= \frac{f_{\text{FPH}}}{2 \times 2^n + 12}
 \end{aligned}$$