

TOSHIBA Microcontrollers
900 Family
(TMP91PW18A) (TMP91CW18A)

October 2004

Datasheet Modifications: I²C Bus Mode Control

The following modifications (shown in red) will be made to the technical datasheets in the next revision.

- In the explanation of the serial bus interface control register 1 in “3.10.4 I²C Bus Mode Control”, “3.11.4 I²C Bus Mode Control”, and “3.12.4 I²C Bus Mode Control”

1. Delete the setting examples where the serial clock frequency exceeds 100 kHz.
2. Add the following note.

Internal serial clock selection <SCK2:0> at write

000	n=5	(Note)	$\left(\begin{array}{l} \text{System clock: } f_c \\ \text{Clock gear: } f_c/1 \\ f_c = 16 \text{ MHz} \\ \text{(internal SCL output)} \\ f_{scl} = \frac{f_c}{2^n + 8} \text{ [Hz]} \end{array} \right)$
001	n=6	- (Note)	
010	n=7	- (Note)	
011	n=8	60.6 kHz	
100	n=9	30.8 kHz	
101	n=10	15.5 kHz	
110	n=11	7.78 kHz	
111		(Reserved)	

Note: This I²C bus circuit does not support the Fast mode. It supports the Standard mode only. Although the I²C bus circuit itself allows the setting of a baud rate over 100 kbps, the compliance with the I²C specification is not guaranteed in that case.

- In “3.10.5 Control in I²C Bus Mode”, “3.11.5 Control in I²C Bus Mode”, and “3.12.5 Control in I²C Bus Mode”

1. Add the following sentence about the communication baud rate.
2. Modify the equations as shown below.

(3) Serial clock

1. Clock source

SBI0CR1X<SCK2:0> is used to specify the maximum transfer frequency for output on the SCL pin in Master mode. **Set a communication baud rate that meets the I²C bus specification, such as the shortest pulse width of t_{LOW}, based on the equations shown below.**

$$\begin{aligned}
 t_{LOW} &= 2^{n-1} / f_{SBI} \\
 t_{HIGH} &= 2^{n-1} / f_{SBI} + 8 / f_{SBI} \\
 f_{scl} &= 1 / (t_{LOW} + t_{HIGH}) \\
 &= \frac{f_{SBI}}{2^n + 8}
 \end{aligned}$$