

**TOSHIBA Microcontrollers**

**870 Family**

(TMP87C409BN) (TMP87C409BM) (TMP87C809BN) (TMP87C809BM) (TMP87P809)  
 (TMP87CH48U) (TMP87CH48DF) (TMP87CM48U) (TMP87CM48DF) (TMP87CH48I)  
 (TMP87PH48U) (TMP87PH48DF) (TMP87PM48U) (TMP87PM48DF)

October 2004

## Datasheet Modifications: I<sup>2</sup>C Bus Mode Control

The following modifications (shown in red) will be made to the technical datasheets in the next revision.

### Section: “I<sup>2</sup>C Bus Mode Control”

▪ **In the explanation of the Serial Bus Interface Control Register 1**

1. Delete the setting examples where the serial clock frequency exceeds 100 kHz.
2. Add the following note.

SCK	Serial clock selection	000 : Reserved (Note)	} at fc = 8MHz (Output on SCL pin)	Write-only
		001 : Reserved (Note)		
		010 : 58.8 kHz		
		011 : 30.3 kHz		
		100 : 15.4 kHz		
		101 : 7.75 kHz		
		110 : 3.89 kHz		
		111 : reserved		

**Note:** This I<sup>2</sup>C bus circuit does not support the Fast mode. It supports the Standard mode only. Although the I<sup>2</sup>C bus circuit itself allows the setting of a baud rate over 100 kbps, the compliance with the I<sup>2</sup>C specification is not guaranteed in that case.

▪ **In “(3) Serial clock”**

1. Add the following sentence about the communication baud rate.

a. Clock source

The SCK (bits 2 to 0 in the SBICR1) is used to select a maximum transfer frequency outputted on the SCL pin in the master mode. **Set a communication baud rate that meets the I<sup>2</sup>C bus specification, such as the shortest pulse width of t<sub>LOW</sub>, based on the equations shown below.**

In both master mode and slave mode, a pulse width of at least 4 machine cycles is require for both “H” and “L” levels.

$$t_{LOW} = 2^n / f_c$$

$$t_{HIGH} = 2^n / f_c + 8 / f_c$$

$$f_{scl} = 1 / (t_{LOW} + t_{HIGH})$$