

Step-Down DC-DC Converter IC Application Notes

Overview

This document provides the usage considerations for Toshiba’s non-isolated step-down DC-DC converters. Before being used, the operations of these converters should be evaluated using actual applications referring to this document.

Non-Isolated Step-Down DC-DC Converters

Principle of Operation

A non-isolated step-down DC-DC converter generates a constant voltage by turning on and off a MOS switch and smoothing an inductor current through an LC filter. The output voltage is determined by its pulse width. The output voltage can therefore be regulated to a desired level by adjusting the pulse width. This operating mode, in which a pulse width is modulated, is called PWM (Pulse Width Modulation) mode. The duty cycle of the operation can be given by:

$$D_{ON} = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

where, V_{IN} = input voltage (V) and V_{OUT} = output voltage (V).

A synchronous rectifier converter, which can be configured by replacing the freewheeling diode D shown in the diagram below with a MOSFET, offers performance characteristics with higher efficiency than the diode rectifier type.

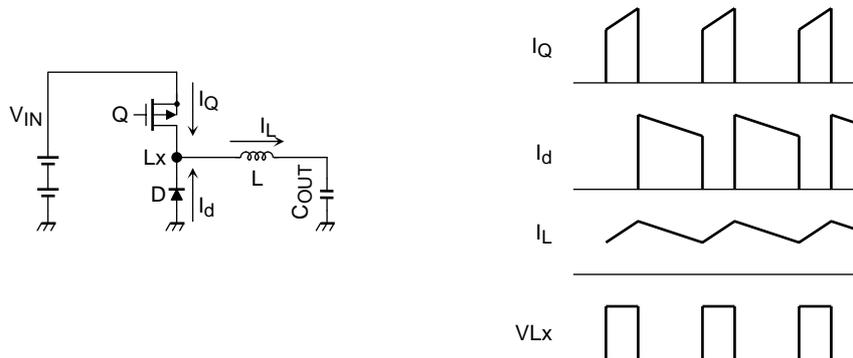


Figure 1 Step-Down DC-DC Converter Circuit and Operating Waveforms

In a DC-DC converter IC, the output voltage is divided by two feedback resistors and applied to the error amplifier. The error amplifier compares the voltage with an internal reference voltage V_{REF} and generates an error voltage. Then, using the error voltage, a PWM signal is generated. This PWM signal controls the on-time and off-time of MOSFETs. The use of negative feedback control, in which an output voltage is fed back to the error amplifier, stabilizes the output voltage of a desired level.

Current-Mode DC-DC Converter

Current-mode control has multiple loops, in which the inductor current is also fed back as well as the output voltage. This control scheme provides the following advantages:

- Simplified phase compensation
- Cycle-by-cycle current limiting
- Improved transient response for load changes
- Improved line regulation

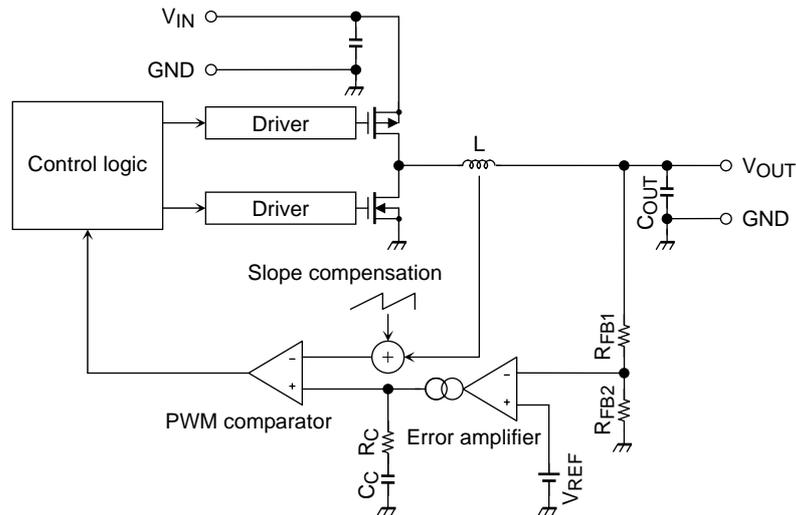


Figure 2 Current-Mode DC-DC Converter

Selecting the Peripheral Components

The following sections describe how to set up each component and also provide general considerations. Since each component should satisfy the control loop requirements, refer to respective datasheets of each device for application circuit examples. At the same time, it should be ensured that the absolute maximum ratings specified by Toshiba are not exceeded during operation.

Inductor

The inductance required to operate a step-down DC-DC converter can be normally calculated by the following equation:

$$L = \frac{V_{IN} - V_{OUT}}{f_{osc} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}} \quad (2)$$

where, V_{IN} = input voltage (V), V_{OUT} = output voltage (V), ΔI_L = inductor ripple current (A) and f_{osc} = oscillation frequency (Hz).

The inductor ripple current (ΔI_L) should be set to 30 to 40% of the maximum output current. When the input voltage (V_{IN}) range of the application set to be used is wide, use the maximum value for V_{IN} in the above equation, so that the (peak) ripple current does not exceed the rated value.

For example, when operating the TB7102F (where oscillation frequency = 1 MHz) at $V_{IN} = 5\text{ V}$, $V_{OUT} = 3.3\text{ V}$ and $I_{OUT} = 1\text{ A}$, ΔI_L should be set to around 0.3 A. L can then be calculated as:

$$L = \frac{V_{IN} - V_{OUT}}{f_{osc} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}} = \frac{5\text{ V} - 3.3\text{ V}}{1\text{ MHz} \cdot 0.3\text{ A}} \cdot \frac{3.3\text{ V}}{5\text{ V}} = 3.7\ \mu\text{H} \quad (3)$$

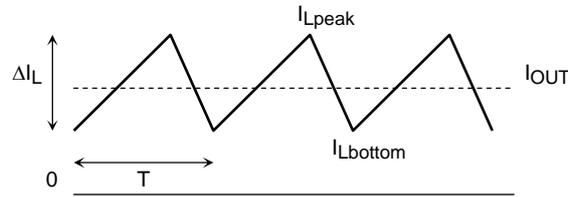


Figure 3 Inductor Current Waveform

The output ripple voltage, ΔV_{OUT} , can be given by:

$$\Delta V_{OUT} = ESR \cdot \Delta I_L \quad (4)$$

where, ESR = equivalent series resistance of the output capacitor (Ω) and ΔI_L = inductor ripple current (A). Thus, to make the output ripple voltage smaller, ESR or ΔI_L should be set smaller. The peak inductor current, I_{Lpeak} is:

$$I_{Lpeak} = I_{OUT} + \frac{1}{2} \cdot \Delta I_L \quad (5)$$

where, I_{OUT} = output current (A) and ΔI_L = inductor ripple current (A).

To prevent an overcurrent limiter from being tripped due to a ripple current, I_{Lpeak} should be set lower than the current limit on the switch pin, I_{LIM} . Also, the rated inductance should be guaranteed even at the peak inductor current, I_{Lpeak} .

Also, to suppress the radiation noise, a closed-magnetic-path inductor should be used. Table 1 shows the relationships between the inductance and various characteristics.

Table 1 Relationships between the Inductance and Various Characteristics

Inductance (L)	Large	↔	Small
Inductor ripple current (ΔI_L)	Small	↔	Large
Peak inductor current (I_{Lpeak})	Low	↔	High
Output ripple voltage (ΔV_{OUT})	Small	↔	Large
Output voltage drop upon sudden load change (ΔV_{drop})	Large	↔	Small
Efficiency (η)	High	↔	Low

Input Capacitor

The ripple current, I_{CINRMS} , which flows through the input capacitor C_{IN} can be calculated as:

$$I_{CINRMS} \approx I_{OUT} \frac{\sqrt{(V_{IN} - V_{OUT}) \cdot V_{OUT}}}{V_{IN}} \quad (6)$$

where, V_{IN} = input voltage (V), V_{OUT} = output voltage (V) and I_{OUT} = output current (A).

The equivalent series resistance (ESR) of the input capacitor causes a power loss. The ripple current rating and allowable ESR of the capacitor to be used should therefore be fully considered.

Sudden load changes should be avoided. Otherwise the charge of C_{IN} might become insufficient upon voltage changes, causing the input voltage to fall below the rated operating voltage. Thus, the input capacitor value should not be too small.

The input capacitor also serves as a bypass capacitor for the internal circuitry. Therefore, its ESR and equivalent series inductance (ESL) should be low enough.

The input ripple voltage, ΔV_{IN} , generated by charging and discharging the input capacitor can be calculated as:

$$\Delta V_{IN} \approx \frac{I_{OUT} \cdot V_{OUT}}{f_{osc} \cdot V_{IN} \cdot C_{IN}} \quad (7)$$

where, V_{IN} = input voltage (V), V_{OUT} = output voltage (V), I_{OUT} = output current (A), f_{osc} = oscillation frequency (Hz) and C_{IN} = input capacitance (F).

When a DC-DC converter is sharing the input voltage of a system with other converters, care should be taken to keep the input ripple voltage small. Otherwise, it can affect the operations of the other converters.

Output Capacitor

The output capacitor, C_{OUT} , greatly affects the output ripple voltage, load transient response and control loop stability.

The output ripple voltage is calculated by Equation 4, $\Delta V_{OUT} = ESR \times \Delta I_L$, which is provided in the Inductor section. Thus, a capacitor with low ESR should be selected to reduce the output ripple voltage.

When the load current in a DC-DC converter suddenly changes, the output voltage decreases at the rate depending on the output capacitor value until the control loop responds. The output capacitor value should therefore be large to reduce the output voltage drop (ΔV_{drop}) due to load changes. At the same time, the output voltage drop calculated as $ESR \times \Delta I_{OUT}$ (ΔI_{OUT} : load variation) also occurs. To reduce such voltage drop, a capacitor with low ESR should be used.

In the case of current-mode DC-DC converters, since the effect of ESR of the output capacitor on the control loop is small, a low-ESR ceramic capacitor can be used. However, the control loop of a DC-DC converter might become unstable if its capacitance is small, while the response speed might become slower if its capacitance is too large. Therefore, refer to respective technical datasheets when selecting an output capacitor.

The ripple current, $I_{COUTRMS}$, which flows through the output capacitor (C_{OUT}) can be calculated as follows:

$$I_{COUTRMS} = \frac{\Delta I_L}{2\sqrt{3}} \quad (8)$$

where, ΔI_L = inductor ripple current (A).

The RMS ripple current through the output capacitor is smaller compared to that through the input capacitor. However, the ESR of the output capacitor, as well as that of the input capacitor, causes a power loss. Thus, the ripple current rating and allowable ESR of the capacitor to be used should be fully considered.

The DC voltage characteristics and temperature characteristics of both the input and output capacitors should be fully considered. The following section provides considerations for each capacitor.

When using ceramic capacitors, their capacitance is greatly affected by the operating supply voltage and temperature. Thus, capacitors with the temperature characteristics of B and x7R should be selected considering the voltage dependence of the capacitance.

When using aluminum electrolytic capacitors, though they can provide large capacitance in spite of their small size, their capacitance and ESR can easily change depending on temperature. Therefore, temperature characteristics of their ESR and capacitance should be evaluated. The reliability also changes over time due to evaporation of the electrolyte, leading to a considerable change in the ESR and capacitance characteristics. Capacitors should therefore be selected considering such reliability change. In recent years, functional polymer capacitors that achieve low ESR while retaining the large capacitance of electrolytic capacitors are available. However, since their withstand voltage is relatively low, care should be taken to avoid overvoltage conditions.

Tantalum capacitors provide large capacitance in spite of their small size, and also provide lower ESR than aluminum electrolytic capacitors. However, since their withstand voltage is relatively low, care should be taken to avoid overvoltage conditions. Also, a breakdown of these capacitors may lead to short circuits. It should therefore be ensured that breakdowns do not occur.

Feed Back Resistors (for Setting the Output Voltage)

The output voltage is set by adjusting the resistive divider ratio of the feedback resistors, R_{FB1} and R_{FB2} , based on the reference voltage of the error amplifier that is connected to the feedback pin. The output voltage can be given by:

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \quad (9)$$

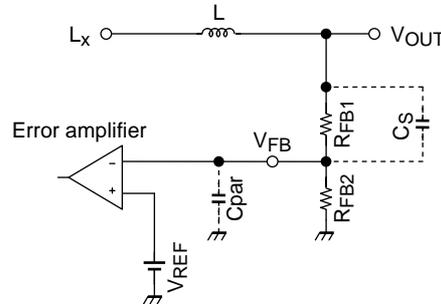


Figure 4 Resistors for Setting the Output Voltage

where, R_{FB1} , R_{FB2} = feedback resistors (Ω) and V_{FB} = feedback pin voltage (V).

The feedback pin has a parasitic capacitance C_{par} . If the R_{FB1} resistor value is extremely high, a delay occurs due to C_{par} at the FB pin, R_{FB1} and R_{FB2} . Refer to the respective datasheet of each device for appropriate resistor values. It is recommended that high-precision resistors with a tolerance of $\pm 1\%$ or lower be used for setting the output voltage.

Also, connecting the C_S capacitor in parallel with R_{FB1} can place a zero (for phase shift reduction) at a frequency calculated by the following equation:

$$f_{cs} = \frac{1}{2\pi \times R_{FB1} \times C_S} \text{ [Hz]} \quad (10)$$

where, R_{FB1} = feedback resistor (Ω) and C_S = feedback capacitor (F).

This helps stabilize the control loop.

Junction Temperature

It should be ensured that the operating junction temperature of the IC (T_{jopr}) does not exceed the absolute maximum rating, considering the ambient temperature (T_a). The junction temperature T_j can be calculated as follows:

$$\begin{aligned} \Delta T_j &= R_{th(j-a)} \times P_{total} \\ T_j &= T_a + \Delta T_j < T_{jopr\ max} \end{aligned} \quad (11)$$

where, ΔT_j = junction temperature rise, $R_{th(j-a)}$ = thermal resistance between junction and ambient; $T_{jopr\ max}$ = maximum rating of the operating junction temperature, T_j = junction temperature, T_a = ambient temperature and P_{total} = power dissipation of the IC.

Printed Circuit Board Layout

To achieve stable operation of a DC-DC converter, a board layout should be carefully designed. Figure 5 shows an application circuit example of the TB7102F. The following provides general considerations for designing a pattern layout taking the TB7102F as an example.

- A DC-DC should be located as close to the loads as possible.
- The bold lines indicate high current traces. They should be as wide as possible.
- The dotted loop ($L_x - L - C_{OUT} - PGND$) indicates a high current path. The traces within the loop should be kept as wide and short as possible to reduce the wiring inductance and resistance, and also to make the loop small.
- Since C_{IN} also serves as a bypass capacitor for the IC, it should be placed as close to the IC as possible. At the same time, the V_{IN} pin should be connected to the power supply without going through through-holes.
- Signal traces for components like R_{FB1} and R_{FB2} should be routed as far away from the inductor and the L_x pin as possible.
- A ground plane is preferred. All the grounds of signal components should be returned to the SGND pin at one point which is then connected to the PGND pin.

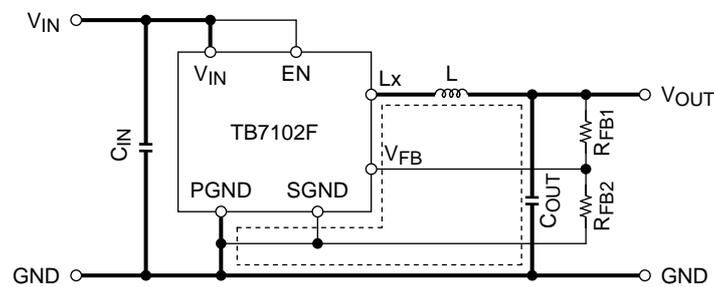


Figure 5 TB7102F Application Circuit Example

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