

# SEMICONDUCTOR GENERAL CATALOG

## ASICs

CMOS Gate Array Series  
CMOS Cell-Based IC Series  
CMOS Embedded Array Series

To ensure competitiveness in the marketplace, companies need to produce more sophisticated, more technology-intensive and higher value-added models, using technological innovation and systematic marketing. Application-specific ICs (ASICs) will give you an edge well beyond your expectations. Toshiba's ASIC offerings include gate arrays, suitable for short delivery times, and cell-based ICs, which enable higher integration with enhanced features, as well as embedded arrays, which have advantages in both development schedules and integration/features. Toshiba will continue to provide ASIC products incorporating leading-edge technologies to pursue new possibilities while meeting an ever-increasing variety of customer needs, appropriately and flexibly.

## Leading-Edge CMOS ASIC Families

< 3 Mixed Power Supply Voltages: Core 1.2 V, I/O 2.5 V/3.3 V, Analog 2.5 V >

### ■ TC320 Series

Fabricated using Toshiba's new CMOS5 65 nanometer process, the high-density low-power TC320 Series combines a low-k dielectric with up to eight levels of copper layer. This new technology offers double the logic density of the CMOS4 process and approx. 30 to 50% reduction in power per gate\*.

In recent years, more accelerated evolution of the broadband network and Internet world pushes the performance levels of data processing components higher, while mobile devices such as cellular phones require power reduction of semiconductor devices to the limit. The TC320 Series is system ASICs ideal for the developments of its successors in a broad range of application fields, delivering high performance required by the network and communication applications; low power consumption required by portable devices; and capability of massive image and audio data processing required by digital multimedia equipment.

The state-of-the-art CMOS5 process technology that permits mixing of logic process, analog and DRAM cores on the same chip allows the world's leading performance in the embedded DRAM ASICs field. Making full use of its accumulated embedded technologies and a variety of IPs, Toshiba strives for better total system solutions.

\* Improvements over the TC300 Series

#### ● Key Features of the TC320 Series

- Sophisticated CMOS process technology
- Stress liner resulting mobility enhancement of transistors
- NIP/SiC coatings technology allowing low sheet resistance
- Advanced optical proximity correction (OPC) technology bringing high-precision microfabrication
- Up to eight levels of copper and one level of Al wiring with low-k dielectric
- Selectable core power voltages: 1.2 V and 1.0 V
- Double the logic density, 15 to 20% reduction in gate delay, 30 to 50% reduction in power per gate
- Supports embedded DRAM
- A variety of high-speed I/Os including serializer/deserializer for chip interfaces
- Short design turn-around-time (TAT) due to the silicon virtual prototyping (SVP)
- Design for manufacturing (DFM) methodology as an answer to manufacturing variance and yield loss
- A variety of packaging for design requiring high-pin-counts, small footprint or low thermal resistance

Process Technology	65-nm process, low-k interlayer dielectric
Gate Length	50 nm
Metal Wiring	Up to 8-layer Cu plus 1-layer Al
Core Supply Voltage	1.2 V/1.0 V (option)
I/O Supply Voltage	1.8 V/2.5 V/3.3 V
Gate Density	800 kgates/mm <sup>2</sup>
Gate Delay	10.2 ps (LP), 7.8 ps (HS)
Power Consumption	5.68 nW/MHz/gate (Fan-out = 0, CQIVX4)

## < Embedded DRAM Cores >

The low-power and high-bandwidth characteristics of Toshiba's embedded DRAM make it ideal for a wide range of applications, including video/image processing devices such as graphics and display controllers; storage devices such as HDD controllers; and digital communication and networking devices.

### Key Features of DRAM Cores

- Much denser than SRAM
- High performance with fast data transfer rates due to wide on-chip memory buses, compared to commodity DRAMs.
- Low power
- Built-in test circuitry and redundancy circuitry
- Flexible core cells generated by a DRAM macro generator

### ■ DRAM Cores for the TC320 Family

The TC320 cell-based ASIC series offers a variety of embedded DRAM cores.

Designers can use the same primitive and I/O cells as well as any IP cores available for the TC320 pure logic process without compromising logic performance.

Characteristics	LP	HS
Max Clock Frequency (Page Mode)	250 MHz	350 MHz
Latency	1, 2, 3	1, 2, 3
Memory Capacity	4 to 32 Mbit	4 to 32 Mbit
Bit Width	64/128/256	256

### ■ DRAM Cores for the TC300 Family

The TC300 cell-based ASIC series offers a variety of embedded DRAM cores.

Designers can use the same primitive and I/O cells as well as any IP cores available for the TC300 pure logic process without compromising logic performance.

Characteristics	SD	SD (LP)*
Random Access Cycle Time	36 ns	40 ns
Latency	1, 2, 3	1, 2, 3
First Data Output Time	—	—
Max Clock Frequency (Page Mode)	222 MHz	200 MHz
Memory Capacity	4 to 32 Mbit	4 to 32 Mbit
Bit Width	64/128/256	64/128/256

\*: The LP version consumes 1/10 the standby current of standard SD macros.

### ■ DRAM Cores for the TC280 Family

The TC280C cell-based ASIC series offers a variety of embedded DRAM cores. Designers can use the same primitive and I/O cells as well as any IP cores available for the TC280C pure logic process without compromising logic performance. The DRAM cores for the TC280 series have the following two types:

1. Standard Synchronous DRAM (SD) macros  
The SD macros are generic DRAM cores, which are available with various bit densities and operate over a wide range of clock frequencies. The SD macros are suitable for applications requiring fast page-mode accesses.
2. Fast-Access (FA) DRAM macros with faster random-access cycle times or data output times  
Toshiba offers two types of FA macros that offer significant advantages over the SD macros in random-access cycle times or data output times:
  - 1) The FA-RC macros have fast random-access cycle times.  
The FA-RC macros are ideal for applications requiring fast random accesses.
  - 2) The FA-AC macros have fast data output times.  
The FA-AC macros also provide fast page-mode accesses.

Characteristics	SD	FA-RC	FA-AC
Random Access Cycle Time	40 ns	10 ns	12 ns
Latency	1, 2, 3	1, 2	2
First Data Output Time	—	14 ns	10 ns
Max Clock Frequency (Page Mode)	200 MHz	—	200 MHz
Memory Capacity	4 to 32 Mbit	2 to 9 Mbit	2 to 9 Mbit
Bit Width	64/128/256	128/144/256/288	128/144/256/288

< Supply Voltage: Single 3.3 V >

■ Advanced 0.3- $\mu$ m, 3-V Low-Voltage ASICs - TC220 Series

- Ultrafast:  
The TC220C cell-based IC Series achieves fast gate delays of just 0.14 ns to 0.15 ns.
- Reduced power consumption:  
The TC220 Series consumes more than 40% less power than the TC200 Series. Power consumption savings of this magnitude are enough to move a design from more expensive ceramic packaging to lower cost plastic packaging. Because customers buying ultraportable devices (such as notebooks and cellular telephones) rank long battery life at the top of their feature preferences, the TC220 Series is ideally suited for these products.
- Available cells:  
Compatible cells such as large SRAMs and ROMs can be integrated on the same chip.

Series	Gate Array	Cell-based IC	Embedded Array
	TC220G	TC220C	TC220E
Process Technology	0.3- $\mu$ m CMOS silicon gate dual/triple-layer metal wiring		
Gate Delay (high drive 2-input NAND gate)	0.15 ns ( $V_{DD} = 3.3$ V, F/O = 2 + Typical Interconnect load)	0.14 ns ( $V_{DD} = 3.3$ V, F/O = 2 + Typical Interconnect load)	0.15 ns ( $V_{DD} = 3.3$ V, F/O = 2 + Typical Interconnect load)
Features	Estimated usable gates (max): 1.9M	High integration RAM/ROM; can accommodate various types of large-capacity cells.	Combines the cell-based IC's extensive libraries of high-performance functions with the gate array advantage of a short production lead time.

< Supply Voltage: Single 5 V >

■ Top-of-the-Line 5-V ASIC - TC190 Series

- High density and low power consumption: with ever increasing levels of integration, total power dissipation may become the limiting feasibility factor. Operating from a single 5-V power supply, the TC190 Series dissipates 45% less power than the TC160 Series, and about 15% less power than the TC170 Series. The TC190 Series is ideally suited for new designs requiring both low power and high density. It supports gate densities of up to 730k.
- PCI local bus interface: PCI is expected to be better suited to the growing challenges of high-speed PCs and workstations due to its design, which is more complex and feature-rich than existing local bus standards. The TC190 Series offers PCI I/O for improved chip-to-chip communication performance.

Series	Gate Array	Cell-based IC
	TC190G	TC190C
Process Technology	0.6- $\mu$ m CMOS silicon gate dual/triple-layer metal wiring	
Gate Delay (high drive 2-input NAND gate)	0.24 ns ( $V_{DD} = 5$ V, F/O = 2 + Typical Interconnect load)	0.22 ns ( $V_{DD} = 5$ V, F/O = 2 + Typical Interconnect load)
Features	Estimated usable gates: 700k gates	High integration RAM/ROM; can accommodate various types of large-capacity cells.

< Supply Voltage: Dual 3.3 V/5 V >

■ 3.3-V/5-V Interface ASIC-TC223 Series

- The TC223 Series operates with a 3-V core and mixed 3-V/5-V I/Os. The 3-V core reduces the power consumption of your design, while the 3-V and 5-V I/O compatibility offers you flexibility in your system interface design. The TC223 Series accomplishes this flexibility by using two power rings for I/O circuitry. One ring is set to operate at 3.3 V and the other at 5 V. There are no restrictions on 3.3-V and 5-V I/O placement. The 3.3-V and 5-V capability also gives you a migration path from mixed 3.3-V/5-V systems to straight 3-V-based systems. Because not all popular ICs have been converted from 5-V to 3-V operation yet, many systems in the near future will be mixed 3.3-V/5-V systems. The TC223 Series makes an ideal interface between 3-V and 5-V circuitry.
- Other features:  
The core of the TC223 series is fabricated using the same dedicated 3.3-volt process as for the TC220 series. The TC223 series thus combines high performance and low power dissipation. The 3.3-volt and 5-volt I/O cells can be freely mixed, giving great flexibility to system design.

Series	Gate Array	Cell-based IC	Embedded Array
	TC223G	TC223C	TC223E
Process Technology	0.3- $\mu$ m CMOS silicon gate dual/triple-layer metal wiring		
Gate Delay (high drive 2-input NAND gate)	0.15 ns ( $V_{DD} = 3.3$ V, F/O = 2 + Typical Interconnect load)	0.14 ns ( $V_{DD} = 3.3$ V, F/O = 2 + Typical Interconnect load)	0.15 ns ( $V_{DD} = 3.3$ V, F/O = 2 + Typical Interconnect load)
Features	Estimated usable gates (max): 1.9M	High integration RAM/ROM; can accommodate various types of large-capacity cells.	Combines the cell-based IC's extensive libraries of high-performance functions with the gate array advantage of a short production lead time.

< Supply Voltage: Dual 2 V/3 V >

Low-Power TC222C Cell-Based IC Series Ideal for Mobile Equipment

Low-Power ASIC:

Fabricated using a 0.3-micron process, the TC222C cell-based IC series is targeted for low-power applications such as mobile equipment. With 2-volt core operation, ultra-low-power cells and power-optimized layout, the TC222C series reduces chip's power dissipation by 70%, as compared to the previous 0.3-micron TC220C series.

Process Technology		0.3 μm HC <sup>2</sup> MOS Si-gate double/triple-layer metal
Gate Delay	2-input NAND, high drive (F/O = 1)	0.10 ns
	2-input NAND, high drive (F/O = 2 + estimated wire load)	0.21 ns
Power Consumption	2-input NAND, low drive (ND2R), (F/O = 1) ♦	0.09 μW/MHz/gate
	2-input NAND, low drive (ND2R), (F/O = 4) ♦	0.18 μW/MHz/gate
Power Supply		[Core] 2.0 V [I/O] 2.0 V/3.0 V
Recommended Operating Voltage Range		[Core] 2.0 V ± 0.2 V [I/O] 2.0 V ± 0.2 V/3.0 V ± 0.3 V

♦: Loaded with low-power cell(s)

Design for Testability

With growing integration densities, test pattern development is taking up an increasing percentage of the time from conception to completion of an ASIC. Internal scan techniques, coupled with ATPG, make it possible to achieve very high fault coverage, approaching 100% on synchronous designs. Toshiba's testability approach saves you the time and effort of designing testability into your ASIC, and allows you to focus on your design efforts rather than on testability issues.

- Toshiba's highly sophisticated software can automatically synthesize test structure, check design rule compliance and generate production test patterns.
- Toshiba also supports a JTAG boundary scan compliant with the IEEE1149.1-1990 standard. BSDL (Boundary Scan Description Language) files may be provided for your board test.

UniversalArray™ QTAT Solution for SoC Designs

The capability to deliver engineering samples at the earliest possible date

What is UniversalArray?

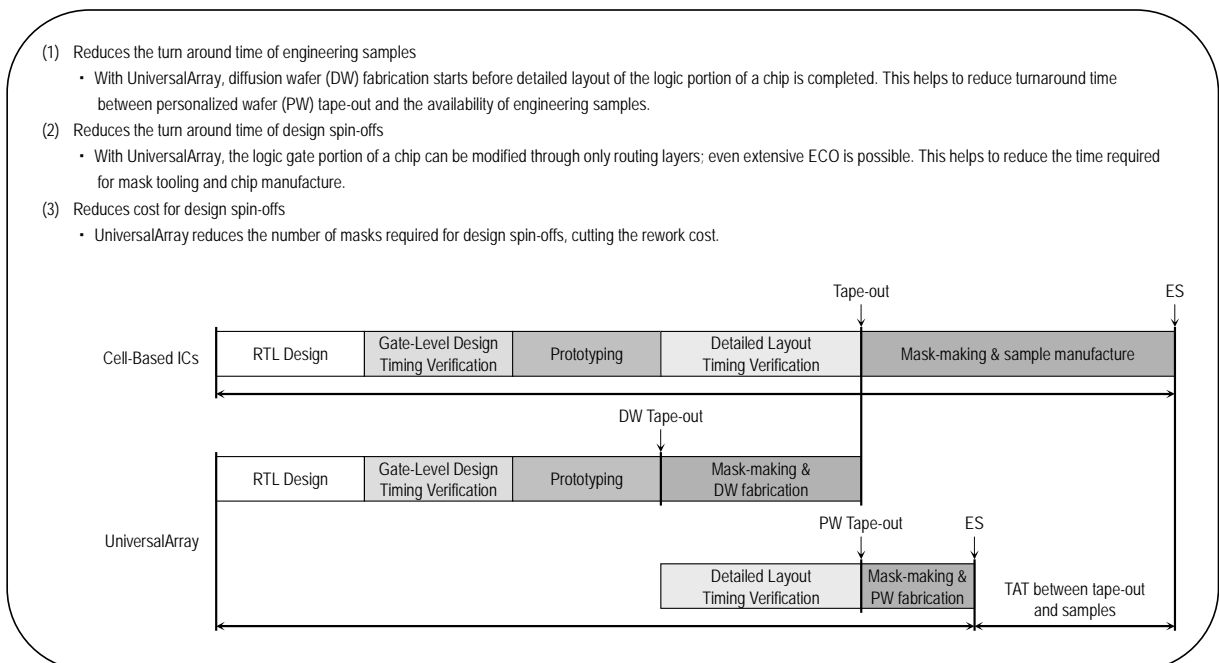
UniversalArray is a new type of cell-based IC platform for the deep-submicron and nanometer devices.

Overview

With SoC design becoming larger and more complex, there is a growing need for a solution that helps reduce time-to-market and development cost. UniversalArray provides an ideal solution.

You can rely on UniversalArray to reduce time-to-market and development cost.

- Design environments that support the 130-nm and 90-nm technologies
  - Provides chip size and performance comparable to cell-based ICs.
  - UniversalArray uses the same cell library as for Toshiba's cell-based ICs.
- UniversalArray Solution



## CMOS Gate Array Series

Gate array wafers may be pre-fabricated in volume up to the final processing steps, thus achieving manufacturing economies of scale.

These wafers are customized at the metal masking stage by applying a unique interconnection pattern that implements the customer's logic design. Therefore, development cost is low and development time is short.

Series	Supply Voltage	Process Technology	Metal Levels	Gate Delay <sup>1)</sup>	Estimated Usable Gates (I/O pads <sup>2)</sup> )
TC220G Series	Single 3.3 V	0.3 $\mu\text{m}$	2, 3	0.15 ns	82,000 (128) to 1,934,000 (512)
TC200G Series		0.4 $\mu\text{m}$	2, 3	0.19 ns	13,000 (80) to 704,000 (512)
TC190G Series	Single 5 V	0.6 $\mu\text{m}$	2, 3	0.24 ns	13,000 (80) to 704,000 (512)
TC223G Series	3.3 V/5 V interface	0.3 $\mu\text{m}$	2, 3	0.15 ns	82,000 (120) to 1,934,000 (504)
TC203G Series	[Core] 3.3 V [I/O] 3.3 V/5 V	0.4 $\mu\text{m}$	2, 3	0.19 ns	19,000 (96) to 694,000 (504)

1) High-drive 2-input NAND gate, Fan-out = 2 plus typical interconnection load

2) When using wire bonding.

- The mixed 3.3/5-volt ASIC series operate with a 3.3-volt core and mixed 3.3/5-volt I/O. The 5-volt I/O cells are designed to tolerate the larger voltage swing of 5-volt signals and are faster than 3.3-volt I/O cells.
- All of the above ASIC series offer megacells, such as high-performance RAMs, ROMs and CPU peripherals.
- Manufactured devices are dry packed, depending on the package used.

## CMOS Cell-Based IC Series

The cell-based technique involves assembly of pre-designed and pre-optimized cells that users select, place and interconnect on-chip to produce the required circuit functions at optimum chip size.

These cells include basic gates, as well as various memory blocks and analog functions. Because all of the mask set needs defining, the development time is longer than for a gate array. However, the density of functions is greater than that achieved by gate arrays.

Series	Supply Voltage	Process Technology	Metal Levels	Gate Delay <sup>1)</sup>	Estimated Usable Gates (I/O pads <sup>2)</sup> )
TC320C Series	2.5 V/3.3 V interface [Core] 1.2 V [I/O] 2.5 V/3.3 V [Analog core] 2.5 V	65 nm	Up to 8-layer Cu plus 1-layer Al	10.2 ps (low power library) 7.8 ps (high-speed library)	Fabricated for each design
TC300C Series	2.5 V/3.3 V interface [Core] 1.2 V [I/O] 2.5 V/3.3 V [Analog core] 2.5 V	90 nm	Up to 11	14 ps (low power library) 11 ps (high-speed library) 9.5 ps (very high-speed library)	Fabricated for each design
TC280C Series	2.5 V/3.3 V interface [Core] 1.5 V [I/O] 2.5 V/3.3 V [Analog core] 2.5 V	0.13 $\mu\text{m}$	4 to 8	59 ps (lower power library) 41 ps (high-speed library) 38 ps (very high-speed library)	Fabricated for each design
TC260C Series	2.5 V/3.3 V interface [Core] 1.5 V [I/O] 2.5 V/3.3 V [Analog core] 2.5 V	0.18 $\mu\text{m}$	3, 4, 5	0.06 ns (low power library) 0.05 ns (high-speed library)	793,000 (156) to 15,955,000 (652)
TC222C Series	2 V/3 V interface [Core] 2 V [I/O] 2 V/3 V	0.3 $\mu\text{m}$	2, 3	0.21 ns	59,000 (96) to 2,077,000 (504)
TC220C Series	Single 3.3 V	0.3 $\mu\text{m}$	2, 3	0.14 ns	59,000 (96) to 2,077,000 (504)
TC200C Series		0.4 $\mu\text{m}$	2, 3	0.17 ns	12,000 (80) to 538,000 (432)
TC190C Series	Single 5 V	0.6 $\mu\text{m}$	2, 3	0.22 ns	12,000 (80) to 538,000 (432)
TC223C Series	3.3 V/5 V interface	0.3 $\mu\text{m}$	2, 3	0.14 ns	59,000 (96) to 2,077,000 (504)
TC203C Series	[Core] 3.3 V [I/O] 3.3 V/5 V	0.4 $\mu\text{m}$	2, 3	0.17 ns	19,000 (96) to 718,000 (504)

1) High-drive 2-input NAND gate, Fan-out = 2 plus typical interconnect load for the other series

4x drive 2-input NAND gate, Fan-out = 1 plus typical interconnect load for TC260C and TC280C.

2) When using wire bonding.

- The TC222C cell-based IC series operates with a 2-volt core and mixed 2/3-volt I/O. The 3-volt I/O cells are designed to tolerate the larger voltage swing of 3-volt signals and are faster than 2-volt I/O cells.
- The mixed 3.3/5-volt ASIC series operate with a 3.3-volt core and mixed 3.3/5-volt I/O. The 5-volt I/O cells are designed to tolerate the larger voltage swing of 5-volt signals and are faster than 3.3-volt I/O cells.
- All of the above ASIC series offer megacells, such as high-performance RAMs, ROMs and CPU peripherals.
- Manufactured devices are dry packed, depending on the package used.

## CMOS Embedded Array Series

The embedded array combines the cell-based IC's extensive libraries of high-performance functions with the gate array advantage of a short production lead time.

Early in the design cycle the appropriate area for gates, embedded memory, core functions, and the number of I/Os are agreed upon by the customer and Toshiba. The customer then continues development work while Toshiba fabricates customer-specific base wafers concurrently. Once the customer completes design, the layout of the gate array portion of the design is performed on the inventoried customer-specific base wafers.

Post-layout simulation is then performed, to verify that the design works to specifications. On customer approval of the design, prototype production can begin with the pre-designed base wafers already waiting at the metal mask step. Toshiba personalizes the base wafers by the use of two or three layers of metallization in much the same way – and as quickly as – fabrication of a gate array. As such, if any design re-spins are necessary, they can be produced with lead times like those of gate arrays.

Series	Supply Voltage	Process Technology	Metal Levels	Gate Delay <sup>1)</sup>	Estimated Usable Gates (I/O pads <sup>2)</sup> )
TC260E Series	2.5 V/3.3 V interface [Core] 1.5 V [I/O] 2.5 V/3.3 V [Analog core] 2.5 V	0.18 $\mu\text{m}$	3, 4, 5	0.06 ns	562,000 (156) to 9,352,000 (652)
TC220E Series	Single 3.3 V	0.3 $\mu\text{m}$	2, 3	0.15 ns	54,000 (104) to 1,934,000 (512)
TC200E Series		0.4 $\mu\text{m}$	2, 3	0.19 ns	13,000 (80) to 503,000 (432)
TC223E Series	3.3 V/5 V interface [Core] 3.3 V [I/O] 3.3 V/5 V	0.3 $\mu\text{m}$	2, 3	0.15 ns	54,000 (96) to 1,934,000 (504)
TC203E Series		0.4 $\mu\text{m}$	2, 3	0.19 ns	19,000 (96) to 694,000 (504)

1) 2-input NAND gate, Fan-out = 2 plus typical interconnection load

4x drive 2-input NAND gate, Fan-out = 1 plus typical interconnect load for TC260E.

2) When using wire bonding.

- The mixed 3.3/5-volt ASIC series operate with a 3.3-volt core and mixed 3.3/5-volt I/O. The 5-volt I/O cells are designed to tolerate the larger voltage swing of 5-volt signals and are faster than 3.3-volt I/O cells.
- Manufactured devices are dry packed, depending on the package used.

**Toshiba America****Electronic Components, Inc.**

- Irvine, Headquarters  
Tel: (949)623-2900 Fax: (949)474-1330
- Buffalo Grove (Chicago)  
Tel: (847)484-2400 Fax: (847)541-7287
- Duluth/Atlanta  
Tel: (770)931-3363 Fax: (770)931-7602
- El Paso  
Tel: (915)771-8156
- Marlborough  
Tel: (508)481-0034 Fax: (508)481-8828
- Parsippany  
Tel: (973)541-4715 Fax: (973)541-4716
- San Jose  
Tel: (408)526-2400 Fax: (408)526-2410
- Wixom (Detroit)  
Tel: (248)347-2607 Fax: (248)347-2602
- Bloomington  
Tel: (952)842-2400 Fax: (952)893-8031
- San Diego  
Tel: (858)385-5900 Fax: (858)674-7606

**Toshiba Electronics do Brasil Ltda.**

Tel: (011)2539-6681 Fax: (011)2539-6675

**Toshiba Electronics Europe GmbH**

- Düsseldorf Head Office  
Tel: (0211)5296-0 Fax: (0211)5296-400
- France Branch  
Tel: (1)47282181
- Italy Branch  
Tel: (039)68701 Fax: (039)6870205
- Spain Branch  
Tel: (91)660-6798 Fax: (91)660-6799
- U.K. Branch  
Tel: (0870)060-2370 Fax: (01252)53-0250
- Sweden Branch  
Tel: (08)704-0900 Fax: (08)80-8459

**Toshiba Electronics Asia (Singapore) Pte. Ltd.**

Tel: (6278)5252 Fax: (6271)5155

**Toshiba Electronics Service (Thailand) Co., Ltd.**

Tel: (02)501-1635 Fax: (02)501-1638

**Toshiba Electronics Trading (Malaysia) Sdn. Bhd.**

- Kuala Lumpur Head Office  
Tel: (03)5631-6311 Fax: (03)5631-6307
- Penang Office  
Tel: (04)226-8523 Fax: (04)226-8515

**Toshiba India Private Ltd.**

Tel: (0124)499-6600 Fax: (0124)499-6611

**Toshiba Electronics Asia, Ltd.**

- Hong Kong Head Office  
Tel: 2375-6111 Fax: 2375-0969
- Beijing Office  
Tel: (010)6590-8796 Fax: (010)6590-8791
- Chengdu Office  
Tel: (028)8675-1773 Fax: (028)8675-1065
- Qingdao Office  
Tel: (532)8579-3328 Fax: (532)8579-3329

**Toshiba Electronics (Shenzhen) Co., Ltd**

Tel: (0755)2399-6897 Fax: (0755)2399-5573

**Toshiba Electronics (Shanghai) Co., Ltd.**

- Shanghai PUXI Branch  
Tel: (021)6139-3888 Fax: (021)6190-8288

- Hangzhou Office  
Tel: (0571)8717-5004 Fax: (0571)8717-5013

- Nanjing Office  
Tel: (025)8689-0070 Fax: (025)8689-0070

**Toshiba Electronics (Dalian) Co., Ltd.**

Tel: (0411)8368-6882 Fax: (0411)8369-0822

**Tsurong Xiamen Xiangyu Trading Co., Ltd.**

Tel: (0592)226-1398 Fax: (0592)226-1399

**Toshiba Electronics Korea Corporation**

- Seoul Head Office  
Tel: (02)3484-4334 Fax: (02)3484-4302
- Daegu Office  
Tel: (053)428-7610 Fax: (053)428-7617

**Toshiba Electronics Taiwan Corporation**

- Taipei Head Office  
Tel: (02)2508-9988 Fax: (02)2508-9999

- ▶ Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
  - ▶ This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
  - ▶ Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
  - ▶ Product is intended for use in general electronics applications (e.g., computers, personal equipment, office equipment, measuring equipment, industrial robots and home electronics appliances) or for specific applications as expressly stated in this document. Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact ("Unintended Use"). Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for Unintended Use unless specifically permitted in this document.
  - ▶ Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
  - ▶ Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
  - ▶ The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
  - ▶ **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
  - ▶ Product may include products using GaAs (Gallium Arsenide). GaAs is harmful to humans if consumed or absorbed, whether in the form of dust or vapor. Handle with care and do not break, cut, crush, grind, dissolve chemically or otherwise expose GaAs in Product.
  - ▶ Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
  - ▶ Product may include products subject to foreign exchange and foreign trade control laws.
  - ▶ Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. TOSHIBA assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
- In addition to the above, the following are applicable only to development tools.
- ▶ Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Use the Product in a way which minimizes risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. For using the Product, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information, including without limitation, this document, the instruction manual, the specifications, the data sheets for Product.
  - ▶ Product is provided solely for the purpose of performing the functional evaluation of a semiconductor product. Please do not use Product for any other purpose, including without limitation, evaluation in high or low temperature or humidity, and verification of reliability.
  - ▶ Do not incorporate Product into your products or system. Products are for your own use and not for sale, lease or other transfer.

**TOSHIBA**