TOSHIBA
Leading Innovation

SEMICONDUCTOR GENERAL CATALOG

ASICs

CMOS Gate Array Series
CMOS Cell-Based IC Series
CMOS Embedded Array Series

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To ensure competitiveness in the marketplace, companies need to produce more sophisticated, more technology-intensive and higher value-added models, using technological innovation and systematic marketing. Application-specific ICs (ASICs) will give you an edge well beyond your expectations. Toshiba's ASIC offerings include gate arrays, suitable for short delivery times, and cell-based ICs, which enable higher integration with enhanced features, as well as embedded arrays, which have advantages in both development schedules and integration/features. Toshiba will continue to provide ASIC products incorporating leading-edge technologies to pursuit new possibilities while meeting an ever-increasing variety of customer needs, appropriately and flexibly.

Leading-Edge CMOS ASIC Families

< 3 Mixed Power Supply Voltages: Core 1.2 V, I/O 2.5 V/3.3 V, Analog 2.5 V >

☐■ TC320 Series

Fabricated using Toshiba's new CMOS5 65 nanometer process, the high-density low-power TC320 Series combines a low-k dielectric with up to eight levels of copper layer. This new technology offers double the logic density of the CMOS4 process and approx. 30 to 50% reduction in power per gate*.

In recent years, more accelerated evolution of the broadband network and Internet world pushes the performance levels of data processing components higher, while mobile devices such as cellular phones require power reduction of semiconductor devices to the limit. The TC320 Series is system ASICs ideal for the developments of its successors in a broad range of application fields, delivering high performance required by the network and communication applications; low power consumption required by portable devices; and capability of massive image and audio data processing required by digital multimedia equipment.

The state-of-the-art CMOS5 process technology that permits mixing of logic process, analog and DRAM cores on the same chip allows the world's leading performance in the embedded DRAM ASICs field. Making full use of its accumulated embedded technologies and a variety of IPs, Toshiba strives for better total system solutions.

* Improvements over the TC300 Series

● Key Features of the TC320 Series

- Sophisticated CMOS process technology
- Stress liner resulting mobility enhancement of transistors
- NiP/SiC coatings technology allowing low sheet resistance
- Advanced optical proximity correction (OPC) technology bringing high-precision microfabrication
- Up to eight levels of copper and one level of Al wiring with low-k dielectric
- Selectable core power voltages: 1.2 V and 1.0 V
- Double the logic density, 15 to 20% reduction in gate delay, 30 to 50% reduction in power per gate
- Supports embedded DRAM
- A variety of high-speed I/Os including serializer/deserializer for chip interfaces
- Short design turn-around-time (TAT) due to the silicon virtual prototyping (SVP)
- Design for manufacturing (DFM) methodology as an answer to manufacturing variance and yield loss
- A variety of packaging for design requiring high-pin-counts, small footprint or low thermal resistance

Process Technology	65-nm process, low-k interlayer dielectric
Gate Length	50 nm
Metal Wiring	Up to 8-layer Cu plus 1-layer Al
Core Supply Voltage	1.2 V/1.0 V (option)
I/O Supply Voltage	1.8 V/2.5 V/3.3 V
Gate Density	800 kgates/mm^2
Gate Delay	10.2 ps (LP), 7.8 ps (HS), 7.2 ps (VS)
Power Consumption	5.68 nW/MHz/gate (Fan-out = 0, CQIVX4)

< Embedded DRAM Cores >

The low-power and high-bandwidth characteristics of Toshiba's embedded DRAM make it ideal for a wide range of applications, including video/image processing devices such as graphics and display controllers; storage devices such as HDD controllers; and digital communication and networking devices.

Key Features of DRAM Cores

- Much denser than SRAM
- High performance with fast data transfer rates due to wide on-chip memory buses, compared to commodity DRAMs.
- Low power
- Built-in test circuitry and redundancy circuitry
- Flexible core cells generated by a DRAM macro generator

☐■ DRAM Cores for the TC320 Family

The TC320 cell-based ASIC series offers a variety of embedded DRAM cores.

Designers can use the same primitive and I/O cells as well as any IP cores available for the TC320 pure logic process without compromising logic performance.

Characteristics	LP	HS
Max Clock Frequency (Page Mode)	250 MHz	350 MHz
Latency	1, 2, 3	1, 2, 3
Memory Capacity	4 to 32 Mbit	4 to 32 Mbit
Bit Width	64/128/256	256

☐■ DRAM Cores for the TC300 Family

The TC300 cell-based ASIC series offers a variety of embedded DRAM cores.

Designers can use the same primitive and I/O cells as well as any IP cores available for the TC300 pure logic process without compromising logic performance.

Characteristics	SD	SD (LP)*
Random Access Cycle Time	36 ns	40 ns
Latency	1, 2, 3	1, 2, 3
First Data Output Time	—	—
Max Clock Frequency (Page Mode)	222 MHz	200 MHz
Memory Capacity	4 to 32 Mbit	4 to 32 Mbit
Bit Width	64/128/256	64/128/256

*: The LP version consumes 1/10 the standby current of standard SD macros.

☐■ DRAM Cores for the TC280 Family

The TC280C cell-based ASIC series offers a variety of embedded DRAM cores. Designers can use the same primitive and I/O cells as well as any IP cores available for the TC280C pure logic process without compromising logic performance. The DRAM cores for the TC280 series have the following two types:

1. FA-RC macros have fast random-access cycle times.
   The FA-RC macros are ideal for applications requiring fast random accesses.
2. FA-AC macros have fast first data output times.
   The FA-AC macros achieve the fast page-mode access.

Characteristics	SD	FA-RC	FA-AC
Random Access Cycle Time	40 ns	10 ns	12 ns
Latency	1, 2, 3	1, 2	2
First Data Output Time	—	14 ns	10 ns
Max Clock Frequency (Page Mode)	200 MHz	—	200 MHz
Memory Capacity	4 to 32 Mbit	2 to 9 Mbit	2 to 9 Mbit
Bit Width	64/128/256	128/144/256/288	128/144/256/288

< Supply Voltage: Single 3.3 V >

☐■ Advanced 0.3-μm, 3-V Low-Voltage ASICs - TC220 Series

- Ultrafast:
  The TC220C cell-based IC Series achieves fast gate delays of just 0.14 ns to 0.15 ns.
- Reduced power consumption:
  The TC220 Series consumes more than 40% less power than the TC200 Series. Power consumption savings of this magnitude are enough to move a design from more expensive ceramic packaging to lower cost plastic packaging. Because customers buying ultraportable devices (such as notebooks and cellular telephones) rank long battery life at the top of their feature preferences, the TC220 Series is ideally suited for these products.
- Available cells:
  Compilable cells such as large SRAMs and ROMs can be integrated on the same chip.

Series	Gate Array	Cell-based IC	Embedded Array
	TC220G	TC220C	TC220E
Process Technology	0.3-μm CMOS silicon gate dual/triple-layer metal wiring		
Gate Delay (high drive 2-input NAND gate)	0.15 ns (V_{DD} = 3.3 V, F/O = 2 + Typical Interconnect load)	0.14 ns (V_{DD} = 3.3 V, F/O = 2 + Typical Interconnect load)	0.15 ns (V_{DD} = 3.3 V, F/O = 2 + Typical Interconnect load)
Features	Estimated usable gates (max): 1.9M	High integration RAM/ROM; can accommodate various types of large-capacity cells.	Combines the cell-based IC's extensive libraries of high-performance functions with the gate array advantage of a short production lead time.

< Supply Voltage: Single 5 V >

☐■ Top-of-the-Line 5-V ASIC - TC190 Series

- High density and low power consumption: with ever increasing levels of integration, total power dissipation may become the limiting feasibility factor. Operating from a single 5-V power supply, the TC190 Series dissipates 45% less power than the TC160 Series, and about 15% less power than the TC170 Series. The TC190 Series is ideally suited for new designs requiring both low power and high density. It supports gate densities of up to 730k.
- PCI local bus interface: PCI is expected to be better suited to the growing challenges of high-speed PCs and workstations due to its design, which is more complex and feature-rich than existing local bus standards. The TC190 Series offers PCI I/O for improved chip-to-chip communication performance.

Series	Gate Array	Cell-based IC
	TC190G	TC190C
Process Technology	0.6-μm CMOS silicon gate dual/triple-layer metal wiring	
Gate Delay (high drive 2-input NAND gate)	0.24 ns (V_{DD} = 5 V, F/O = 2 + Typical Interconnect load)	0.22 ns (V_{DD} = 5 V, F/O = 2 + Typical Interconnect load)
Features	Estimated usable gates: 700k gates	High integration RAM/ROM; can accommodate various types of large-capacity cells.

< Supply Voltage: Dual 3.3 V/5 V >

☐■ 3.3-V/5-V Interface ASIC-TC223 Series

- The TC223 Series operates with a 3-V core and mixed 3-V/5-V I/Os. The 3-V core reduces the power consumption of your design, while the 3-V and 5-V I/O compatibility offers you flexibility in your system interface design. The TC223 Series accomplishes this flexibility by using two power rings for I/O circuitry. One ring is set to operate at 3.3 V and the other at 5 V. There are no restrictions on 3.3-V and 5-V I/O placement. The 3.3-V and 5-V capability also gives you a migration path from mixed 3.3-V/5-V systems to straight 3-V-based systems. Because not all popular ICs have been converted from 5-V to 3-V operation yet, many systems in the near future will be mixed 3.3-V/5-V systems. The TC223 Series makes an ideal interface between 3-V and 5-V circuitry.
- Other features:
  The core of the TC223 series is fabricated using the same dedicated 3.3-volt process as for the TC220 series. The TC223 series thus combines high performance and low power dissipation. The 3.3-volt and 5-volt I/O cells can be freely mixed, giving great flexibility to system design.

Series	Gate Array	Cell-based IC	Embedded Array
	TC223G	TC223C	TC223E
Process Technology	0.3-μm CMOS silicon gate dual/triple-layer metal wiring		
Gate Delay (high drive 2-input NAND gate)	0.15 ns (V_{DD} = 3.3 V, F/O = 2 + Typical Interconnect load)	0.14 ns (V_{DD} = 3.3 V, F/O = 2 + Typical Interconnect load)	0.15 ns (V_{DD} = 3.3 V, F/O = 2 + Typical Interconnect load)
Features	Estimated usable gates (max): 1.9M	High integration RAM/ROM; can accommodate various types of large-capacity cells.	Combines the cell-based IC's extensive libraries of high-performance functions with the gate array advantage of a short production lead time.

< Supply Voltage: Dual 2 V/3 V >

☐■ Low-Power TC222C Cell-Based IC Series Ideal for Mobile Equipment

・ Low-Power ASIC:
Fabricated using a 0.3-micron process, the TC222C cell-based IC series is targeted for low-power applications such as mobile equipment. With 2-volt core operation, ultra-low-power cells and power-optimized layout, the TC222C series reduces chip's power dissipation by 70%, as compared to the previous 0.3-micron TC220C series.

Process Technology		0.3 μm HC^2MOS Si-gate double/triple-layer metal
Gate Delay	2-input NAND, high drive (F/O = 1)	0.10 ns
	2-input NAND, high drive (F/O = 2 + estimated wire load)	0.21 ns
Power Consumption	2-input NAND, low drive (ND2R), (F/O = 1) ♦	0.09 μW/MHz/gate
	2-input NAND, low drive (ND2R), (F/O = 4) ♦	0.18 μW/MHz/gate
Power Supply		[Core] 2.0 V [I/O] 2.0 V/3.0 V
Recommended Operating Voltage Range		[Core] 2.0 V ± 0.2 V [I/O] 2.0 V ± 0.2 V/3.0 V ± 0.3 V

♦: Loaded with low-power cell(s)

Design for Testability

With growing integration densities, test pattern development is taking up an increasing percentage of the time from conception to completion of an ASIC. Internal scan techniques, coupled with ATPG, make it possible to achieve very high fault coverage, approaching 100% on synchronous designs. Toshiba's testability approach saves you the time and effort of designing testability into your ASIC, and allows you to focus on your design efforts rather than on testability issues.

・ Toshiba's highly sophisticated software can automatically synthesize test structure, check design rule compliance and generate production test patterns.

・ Toshiba also supports a JTAG boundary scan compliant with the IEEE1149.1-1990 standard. BSDL (Boundary Scan Description Language) files may be provided for your board test.

UniversalArray™ QTAT Solution for SoC Designs

The capability to deliver engineering samples at the earliest possible date

■ What is UniversalArray?
UniversalArray is a new type of cell-based IC platform for the deep-submicron and nanometer devices.

■ Overview
With SoC design becoming larger and more complex, there is a growing need for a solution that helps reduce time-to-market and development cost. UniversalArary provides an ideal solution.

<u>You can rely on UniversalArray to reduce time-to-market and development cost.</u>

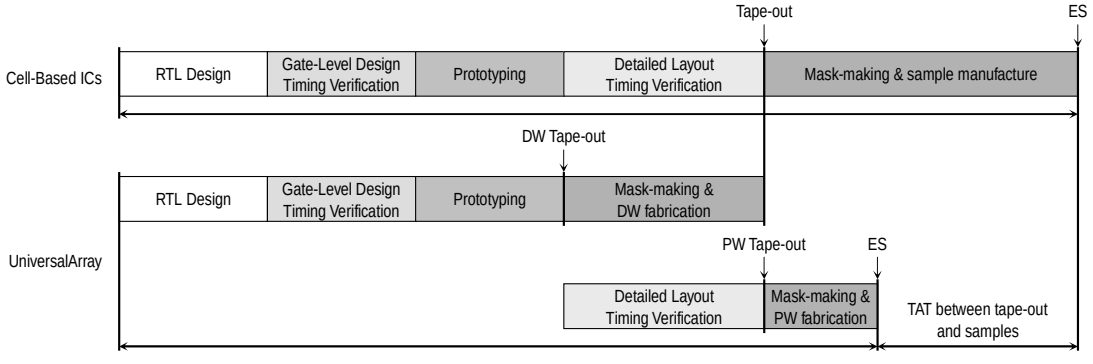
- Design environment tailored to the state-of-the-art processes
  Supports 130- and 90-nm technology nodes.
- Provides chip size and performance comparable to cell-based ICs.
- UniversalArray uses the same cell library as for Toshiba's cell-based ICs.

■ UnivseralArray Solution

(1) Reduces the turn around time of engineering samples
・ With UniversalArray, diffusion wafer (DW) fabrication starts before detailed layout of the logic portion of a chip is completed. This helps to reduce turnaround time between personalized wafer (PW) tape-out and the availability of engineering samples.

(2) Reduces the turn around time of design spin-offs
・ With UniversalArray, the logic gate portion of a chip can be modified through only routing layers; even extensive ECO is possible. This helps to reduce the time required for mask tooling and chip manufacture.

(3) Reduces cost for design spin-offs
・ UniversalArray reduces the number of masks required for design spin-offs, cutting the rework cost.



CMOS Gate Array Series

Gate array wafers may be pre-fabricated in volume up to the final processing steps, thus achieving manufacturing economies of scale.
These wafers are customized at the metal masking stage by applying a unique interconnection pattern that implements the customer's logic design. Therefore, development cost is low and development time is short.

Series	Supply Voltage	Process Technology	Metal Levels	Gate Dalay[1)]	Estimated Usable Gates (I/O pads[2)])
TC220G Series	Single 3.3 V	0.3 μm	2, 3	0.15 ns	82,000 (128) to 1,934,000 (512)
TC200G Series		0.4 μm	2, 3	0.19 ns	13,000 (80) to 704,000 (512)
TC190G Series	Single 5 V	0.6 μm	2, 3	0.24 ns	13,000 (80) to 704,000 (512)
TC223G Series	3.3 V/5 V interface	0.3 μm	2, 3	0.15 ns	82,000 (120) to 1,934,000 (504)
TC203G Series	[Core] 3.3 V [I/O] 3.3 V/5 V	0.4 μm	2, 3	0.19 ns	19,000 (96) to 694,000 (504)

1) High-drive 2-input NAND gate, Fan-out = 2 plus typical interconnection load
2) When using wire bonding.

- The mixed 3.3/5-volt ASIC series operate with a 3.3-volt core and mixed 3.3/5-volt I/O. The 5-volt I/O cells are designed to tolerate the larger voltage swing of 5-volt signals and are faster than 3.3-volt I/O cells.
- All of the above ASIC series offer megacells, such as high-performance RAMs, ROMs and CPU peripherals.
- Manufactured devices are dry packed, depending on the package used.

CMOS Cell-Based IC Series

The cell-based technique involves assembly of pre-designed and pre-optimized cells that users select, place and interconnect on-chip to produce the required circuit functions at optimum chip size.
These cells include basic gates, as well as various memory blocks and analog functions. Because all of the mask set needs defining, the development time is longer than for a gate array. However, the density of functions is greater than that achieved by gate arrays.

Series	Supply Voltage	Process Technology	Metal Levels	Gate Dalay[1)]	Estimated Usable Gates (I/O pads[2)])
TC320C Series	2.5 V/3.3 V interface [Core] 1.2 V [I/O] 2.5 V/3.3 V [Analog core] 2.5 V	65 nm	Up to 8-layer Cu plus 1-layer Al	14 ps (low power library) 11 ps (high-speed library)	Fabricated for each design
TC300C Series	2.5 V/3.3 V interface [Core] 1.2 V [I/O] 2.5 V/3.3 V [Analog core] 2.5 V	90 nm	Up to 11	14 ps (low power library) 11 ps (high-speed library) 9.5 ps (very high-speed library)	Fabricated for each design
TC280C Series	2.5 V/3.3 V interface [Core] 1.5 V [I/O] 2.5 V/3.3 V [Analog core] 2.5 V	0.13 μm	4 to 8	59 ps (lower power library) 41 ps (high-speed library) 38 ps (very high-speed library)	Fabricated for each design
TC260C Series	2.5 V/3.3 V interface [Core] 1.5 V [I/O] 2.5 V/3.3 V [Analog core] 2.5 V	0.18 μm	3, 4, 5	0.06 ns (low power library) 0.05 ns (high-speed library)	793,000 (156) to 15,955,000 (652)
TC222C Series	2 V/3 V interface [Core] 2 V [I/O] 2 V/3 V	0.3 μm	2, 3	0.21 ns	59,000 (96) to 2,077,000 (504)
TC220C Series	Single 3.3 V	0.3 μm	2, 3	0.14 ns	59,000 (96) to 2,077,000 (504)
TC200C Series		0.4 μm	2, 3	0.17 ns	12,000 (80) to 538,000 (432)
TC190C Series	Single 5 V	0.6 μm	2, 3	0.22 ns	12,000 (80) to 538,000 (432)
TC223C Series	3.3 V/5 V interface	0.3 μm	2, 3	0.14 ns	59,000 (96) to 2,077,000 (504)
TC203C Series	[Core] 3.3 V [I/O] 3.3 V/5 V	0.4 μm	2, 3	0.17 ns	19,000 (96) to 718,000 (504)

1) High-drive 2-input NAND gate, Fan-out = 2 plus typical interconnect load for the other series
4x drive 2-input NAND gate, Fan-out = 1 plus typical interconnect load for TC260C and TC280C.
2) When using wire bonding.

- The TC222C cell-based IC series operates with a 2-volt core and mixed 2/3-volt I/O. The 3-volt I/O cells are designed to tolerate the larger voltage swing of 3-volt signals and are faster than 2-volt I/O cells.
- The mixed 3.3/5-volt ASIC series operate with a 3.3-volt core and mixed 3.3/5-volt I/O. The 5-volt I/O cells are designed to tolerate the larger voltage swing of 5-volt signals and are faster than 3.3-volt I/O cells.
- All of the above ASIC series offer megacells, such as high-performance RAMs, ROMs and CPU peripherals.
- Manufactured devices are dry packed, depending on the package used.

CMOS Embedded Array Series

The embedded array combines the cell-based IC's extensive libraries of high-performance functions with the gate array advantage of a short production lead time.
Early in the design cycle the appropriate area for gates, embedded memory, core functions, and the number of I/Os are agreed upon by the customer and Toshiba. The customer then continues development work while Toshiba fabricates customer-specific base wafers concurrently. Once the customer completes design, the layout of the gate array portion of the design is performed on the inventoried customer-specific base wafers.
Post-layout simulation is then performed, to verify that the design works to specifications. On customer approval of the design, prototype production can begin with the pre-designed base wafers already waiting at the metal mask step. Toshiba personalizes the base wafers by the use of two or three layers of metallization in much the same way – and as quickly as – fabrication of a gate array. As such, if any design re-spins are necessary, they can be produced with lead times like those of gate arrays.

Series	Supply Voltage	Process Technology	Metal Levels	Gate Dalay[1)]	Estimated Usable Gates (I/O pads[2)])
TC260E Series	2.5 V/3.3 V interface [Core] 1.5 V [I/O] 2.5 V/3.3 V [Analog core] 2.5 V	0.18 μm	3, 4, 5	0.06 ns	562,000 (156) to 9,352,000 (652)
TC220E Series	Single 3.3 V	0.3 μm	2, 3	0.15 ns	54,000 (104) to 1,934,000 (512)
TC200E Series		0.4 μm	2, 3	0.19 ns	13,000 (80) to 503,000 (432)
TC223E Series	3.3 V/ 5 V interface [Core] 3.3 V [I/O] 3.3 V/5 V	0.3 μm	2, 3	0.15 ns	54,000 (96) to 1,934,000 (504)
TC203E Series		0.4 μm	2, 3	0.19 ns	19,000 (96) to 694,000 (504)

1) 2-input NAND gate, Fan-out = 2 plus typical interconnection load
4x drive 2-input NAND gate, Fan-out = 1 plus typical interconnect load for TC260E.
2) When using wire bonding.

- The mixed 3.3/5-volt ASIC series operate with a 3.3-volt core and mixed 3.3/5-volt I/O. The 5-volt I/O cells are designed to tolerate the larger voltage swing of 5-volt signals and are faster than 3.3-volt I/O cells.
- Manufactured devices are dry packed, depending on the package used.

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